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EXAMINER	
TRIMMINGS, JOHN P	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 04/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/679,266	MANTRI, PRASAD	
	Examiner	Art Unit	
	John P. Trimmings	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-44* is/are rejected.

7)☒ Claim(s) *24-43* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/7/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-44 are presented for examination.

Information Disclosure Statement

1. The examiner has considered the applicant's Information Disclosure Stetement dated 10/07/2003.

Drawings

2. The drawings are objected to because:

FIG.1 "P#" should be corrected to, "D#".

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the

applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The abstract of the disclosure is objected to because line 5 of the paragraph should be corrected to read, "... can also be ~~repair~~ repaired or disabled ...". Correction is required. See MPEP § 608.01(b).

4. The disclosure is objected to because of the following informalities:

a. Paragraph [0008] is objected to because it describes a no-match" condition (in line 3) as pulling the line ML to ground (a "0"). But FIG.1 as drawn depicts a "no-match" as line ML being at pre-charge potential (a "1"). And, FIG.1 depicts a "match" as pulling line ML to ground ("0"), therefore, the examiner requests the applicant to change the paragraph to match the drawing of FIG.1. Appropriate correction is required.

b. Paragraph [0010] is objected to because the sentence beginning on line 6 ("In this manner ...") should describe the pulling down of line ML if the search data SD matches at node D, "or" (not "and") if the search data SD# matches the complement of node D, in order to be in agreement with the circuit as drawn.

Therefore the correction for line 8 of the paragraph 10 should be as follows; "... the data stored at node D ~~and~~ or the complement of the search data on line SD# ...".

c. Paragraph [0010] is objected to because the last line of the paragraph describes the pre-charge level to be a "match" condition, which is in contradiction to the sentence beginning on line 6 of the same paragraph.

d. Paragraph [0023] is objected to because line 6 should be corrected to read, "... mask M of each is set to a not mask state ...".

e. Paragraph [0023] is objected to because the last sentence (This ensures ...") contradicts the teaching of FIG.1 where the sentence states that "pull down" of a match line occurs during a mismatch, because the drawing of FIG.1 teaches that "pull down" of a match line occurs during a match.

f. Paragraph [0025] is objected to because line 6 should instead read, "... bit in the search pattern is the complement of ...".

g. Paragraph [0025] is objected to because line 7, "... is set to equal as corresponding pattern i.". The examiner requests that the phrase be reworded to clearly state that bit-i is different.

h. Paragraph [0025] is objected to because line 7 describes a "walking 0" pattern for the search key, but the pattern is instead a walking 1" pattern.

i. Paragraph [0029] is objected to because line 4 describes a "walking 1" pattern for the search key, but the pattern is instead a walking 0" pattern.

Claim Objections

5. Claims 24-43 are objected to because of the following informalities:

The examiner requests that each claim, 1st line, be changed to read, "... at least one signal ~~by~~ comprises:".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 1, 23 and 44 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claims contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The claims, limiting the CAM test to a test that detects weak match lines, are supported by a disclosure (paragraphs [0024] through [0029]), and a drawing (FIG.5) that is not enabling. The recital of the test procedure, and the supporting FIG.5 fail to enable anyone with ordinary skill in the art to perform a test for a weak pull-down match line. The disclosure describes, and the figure supports at "START", a CAM data full of all 1's (11...11), and a search key of a walking-1 pattern (beginning with 10...00). Such a test should cause a failure if the pull-down fails to a no-match state, but the disclosure and the drawing of the method in FIG.5 both fail to disclose this result. Since both disclosure and drawing have failed to teach the test, the examiner presumes that the

inventor was not in possession of the essentials of the test, and has failed to enable "weak pull-down" testing.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 16 and 37 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claims attempt to limit the claims to detection of an M2 short condition, but have instead described an M1# open, M3 open, M2# open, SD#, and ML failure instead. The examiner is unsure of what the applicant intends to claim in these claims, and so the claims are indefinite.

8. Claims 21 and 42 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claims attempt to limit the claims to detection of an M3 short condition, but have instead described an M2# short, M1 short, SD#, and ML failure instead. The examiner is unsure of what the applicant intends to claim in these claims, and so the claims are indefinite.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1, 2, 4-18 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhao et al., (herein Zhao #1), "Testing SRAM-Based Content Addressable Memories", in view of Zhao et al. (herein Zhao #2), U.S. Patent No. 6496950, and further in view of Patel, "Circuits for Low Power Traffic Encoding".

As per Claims 1 and 44:

Zhao #1 teaches a system or method for testing a plurality of content addressable memory (CAM) cells in a CAM device (see Title), comprising the means/steps of: (a) testing said CAM device for stuck match lines (see page 1061, pass 3 and page 1062 column 1 bullet 5 or column 2 bullet 9); but is not very specific about testing for weak pull-downs. But in the analogous art of Zhao #2, the feature is disclosed, wherein there is (b) testing said CAM device for weak-pull down lines (see column 13 lines 50-67 and column 14 lines 1-22); and further, (c) testing each CAM cell in said CAM device to locate a faulty CAM cell (column 14 lines 54-67 and column 15 lines 1-22); but Zhao #2 fails to further teach diagnosing faults. But Zhao #1 further teaches this feature wherein (d) for each faulty CAM cell identified in step (c) (comparison related faults, page 1057 column 1 4.2 1st paragraph), diagnosing a cause of fault for said faulty CAM cell by applying at least one signal and reading a state of a match line associated with said faulty cell (see Tables 2 and 3 on page 1058). The examiner, being one of ordinary skill, recognizes the difference between the above references and the application to be simply a difference between the level of the match

line (ML) under the test condition of a "match": The references teach that ML=1=Match, but this application teaches that ML=0=Match. But such a difference is an obvious alternative choice of design (see Patel on page 4 column 1 last paragraph). Therefore, no differences exist between the references and the application, when viewed in light of such a design choice. And in Zhao #1, the Abstract cites an advantage to be complete characterization of comparison faults is attained by analysis of the circuit structure. In Patel, the design choice is driven (page 4 column 1 last paragraph) by a choice of using ML=0=Match to conserve power. One with ordinary skill in the art at the time of the invention, motivated as suggested, would have found it obvious to use the design choice of ML=0=Match (in Patel) to conserve power, and to use the diagnosis tables of Zhao #1 in order to improve test results in Zhao #2.

As per Claim 2:

Zhao #1 further teaches the method of claim 1, wherein step (c) is performed after both steps (a) and (b), and step (d) is performed after step (c). The method is rejected based on Zhao #1 where step (c) is performed after step (a) (see Zhao #1, page 1060 where test (a) is the 1st test to be executed, pass 1 to pass 3), as well as step (b) which is not enabled (see 112 rejection above). And, the diagnosing of faults (d) occurs during and after pass 3 (see page 1060). And in view of the motivation previously stated, the claim is rejected.

As per Claim 4:

Zhao #1 Table 3 teaches the method of claim 1, wherein said step of applying at least one signal comprises: setting a storage location of said faulty CAM cell to a logical

zero; setting a search data line of said faulty CAM cell to a logical one; setting a complement search data line of said faulty CAM cell to a logical zero; and identifying a faulty match line if said match line is set to logical zero (Table 3 ML S-A-0 line 2).

NOTE: In view of the design choice where ML=0=Match is chosen (see Claim 1 above), the references used in Zhao #1 Table 3 are equivalent to the applicant's Table 1 as follows:

S = D in applicant's Table 1.

S' = D# in applicant's Table 1.

CBL' = SD in applicant's Table 1 (Complementing enables ML=0=Match).

CBL = SD# in applicant's Table 1 (Complementing enables ML=0=Match).

ML Good/Fail = ML Fault-Free/Faulty in applicant's Table 1.

In view of the applicant's paragraphs [0009] and [0010], the Mask register is assumed on all the time when testing faults, and thus the binary CAM in Zhao #1 applies in such a case. And in view of the motivation and design choice previously stated, the claim is rejected.

As per Claim 5:

Zhao #1 Table 3 further teaches the method of claim 1, wherein said step of applying at least one signal comprises: setting a storage location of said faulty CAM cell to a logical one; setting a search data line of said faulty CAM cell to a logical zero; setting a complement search data line of said faulty CAM cell to a logical one; and identifying a faulty match line if said match line is set to logical zero (Table 3 ML S-A-0

line 1). And in view of the motivation and design choice previously stated, the claim is rejected.

As per Claim 6:

Zhao #1 Table 3 further teaches the method of claim 1, wherein said step of applying at least one signal comprises: setting a storage location of said faulty CAM cell to a logical zero; setting a mask value of said faulty CAM cell to a logical one; setting a search data line of said faulty CAM cell to a logical zero; setting a complement search data line of said faulty CAM cell to a logical one; and identifying a faulty match line if said match line is set to logical one (Table 3 ML S-A-1 line 2). And in view of the motivation and design choice previously stated, the claim is rejected.

As per Claim 7:

Zhao #1 Table 3 further teaches the method of claim 1, wherein said step of applying at least one signal comprises: setting a storage location of said faulty CAM cell to a logical one; setting a mask value of said faulty CAM cell to a logical one; setting a search data line of said faulty CAM cell to a logical one; setting a complementary search data line of said faulty CAM cell to a logical zero; and identifying a faulty search data line if said match line is set to logical one (Table 3 CBL' S-A-0). And in view of the motivation and design choice previously stated, the claim is rejected.

As per Claim 8:

Zhao #1 Table 3 further teaches the method of claim 1, wherein said step of applying at least one signal comprises: setting a storage location of said faulty CAM cell to a logical one; setting a mask value of said faulty CAM cell to a logical one; setting a

search data line of said faulty CAM cell to a logical zero; setting a complementary search data line of said faulty CAM cell to a logical one; and identifying a faulty search data line if said match line is set to logical zero (Table 3 CBL' S-A-1). And in view of the motivation and design choice previously stated, the claim is rejected.

As per Claim 9:

Zhao #1 Table 3 further teaches the method of claim 1, wherein said step of applying at least one signal comprises: setting a storage location of said faulty CAM cell to a logical zero; setting a mask value of said faulty CAM cell to a logical one; setting a search data line of said faulty CAM cell to a logical zero; setting a complementary search data line of said faulty CAM cell to a logical one; and identifying a faulty complement search data line if said match line is set to a logical one (Table 3 CBL S-A-0). And in view of the motivation and design choice previously stated, the claim is rejected.

As per Claim 10:

Zhao #1 Table 3 further teaches the method of claim 1, wherein said step of applying at least one signal comprises: setting a storage location of said faulty CAM cell to a logical zero; setting a mask value of said faulty CAM cell to a logical one; setting a search data line of said faulty CAM cell to a logical one; setting a complementary search data line of said faulty CAM cell to a logical zero; and identifying a faulty complement search data line if said match line is set to logical zero (Table 3 CBL S-A-1). And in view of the motivation and design choice previously stated, the claim is rejected.

As per Claim 11:

Zhao #1 Table 3 further teaches the method of claim 1, wherein said step of applying at least one signal comprises: setting a storage location of said faulty CAM cell to a logical one; setting a mask value of said faulty CAM cell to a logical one; setting a search data line of said faulty CAM cell to a logical one; setting a complementary search data line of said faulty CAM cell to a logical zero; and identifying an stuck open fault with a transistor having a gate coupled to a data storage node of said CAM cell, if said match line is set to logical one (M_2 S-Open line 1). And in view of the motivation and design choice previously stated, the claim is rejected.

As per Claim 12:

Zhao #1 Table 3 further teaches the method of claim 1, wherein said step of applying at least one signal comprises: setting a storage location of said faulty CAM cell to a logical zero; setting a mask value of said faulty CAM cell to a logical one; setting a search data line of said faulty CAM cell to a logical one; setting a complementary search data line of said faulty CAM cell to a logical zero; and identifying an short circuit fault with a transistor having a gate coupled to a data storage node of said CAM cell, if said match line is set to logical zero (M_2 S-On line 1). And in view of the motivation and design choice previously stated, the claim is rejected.

As per Claim 13:

Zhao #1 Table 3 further teaches the method of claim 1, wherein said step of applying at least one signal comprises: setting a storage location of said faulty CAM cell to a logical zero; setting a mask value of said faulty CAM cell to a logical one; setting a search data line of said faulty CAM cell to a logical zero; setting a complementary

search data line of said faulty CAM cell to a logical one; and identifying an stuck open fault with a transistor having a gate coupled to a complement of a data storage node if said match line is set to a logical one (M_1 S-Open line 2). And in view of the motivation and design choice previously stated, the claim is rejected.

As per Claim 14:

Zhao #1 Table 3 further teaches the method of claim 1, wherein said step of applying at least one signal comprises: setting a storage location of said faulty CAM cell to a logical one; setting a mask value of said faulty CAM cell to a logical one; setting a search data line of said faulty CAM cell to a logical zero; setting a complementary search data line of said faulty CAM cell to is set to a logical one; and identifying a short circuit fault with a transistor having a gate coupled to a complement of a data storage node, if said match line is set to logical zero (M_1 S-On line 2). And in view of the motivation and design choice previously stated, the claim is rejected.

As per Claim 15:

Zhao #1 Table 3 further teaches the method of claim 1, wherein said step of applying at least one signal comprises: setting a storage location of said faulty CAM cell to a logical zero; setting a mask value of said faulty CAM cell to a logical one; setting a search data line of said faulty CAM cell to a logical zero; setting a complementary search data line of said faulty CAM cell to a logical one; and identifying a stuck open fault with a transistor having a gate coupled to a search data line, if said match line is set to logical one (M_2 S-On line 2). And in view of the motivation and design choice previously stated, the claim is rejected.

As per Claim 16:

Zhao #1 Table 3 further teaches the method of claim 1, wherein said step of applying at least one signal comprises: setting a storage location of said faulty CAM cell to a logical zero; setting a mask value of said faulty CAM cell to a logical one; setting a search data line of said faulty CAM cell to a logical zero; setting a complementary search data line of said faulty CAM cell to a logical one; and identifying a short circuit fault with a transistor having a gate coupled to a search data line, if said match line is set to logical one (M_1 S-On line 1). And in view of the motivation and design choice previously stated, the claim is rejected.

As per Claim 17:

Zhao #1 Table 3 further teaches the method of claim 1, wherein said step of applying at least one signal comprises: setting a storage location of said faulty CAM cell to a logical zero; setting a mask value of said faulty CAM cell to a logical one; setting a search data line of said faulty CAM cell to a logical zero; setting a complementary search data line of said faulty CAM cell to a logical one; and identifying a stuck open fault with a transistor having a gate coupled to a complementary search data line, if said match line is set to one (M_1 S-Open line 2). And in view of the motivation and design choice previously stated, the claim is rejected.

As per Claim 18:

Zhao #1 Table 3 further teaches the method of claim 1, wherein said step of applying at least one signal comprises: setting a storage location of said faulty CAM cell to a logical zero; setting a mask value of said faulty CAM cell to a logical one; setting a

search data line of said faulty CAM cell to a logical one; setting a complementary search data line of said faulty CAM cell to a logical zero; and identifying a short circuit fault with a transistor having a gate coupled to a complementary search data line, if said match line is set to logical zero (M_2 S-On line 1). And in view of the motivation and design choice previously stated, the claim is rejected.

11. Claims 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhao et al., (herein Zhao #1), "Testing SRAM-Based Content Addressable Memories", in view of Zhao et al. (herein Zhao #2), U.S. Patent No. 6496950, in view of Patel, "Circuits for Low Power Traffic Encoding" as applied to Claim 1 above, and further in view of Wright et al. (herein Wright), "Transistor-Level Fault Analysis and Test Algorithm Development for Ternary Dynamic Content Addressable Memories".

As per Claim 19:

Zhao #1 Table 3 further teaches the method of claim 1, wherein said step of applying at least one signal comprises: setting a storage location of said faulty CAM cell to a logical one; setting a mask value of said faulty CAM cell to a logical one; setting a search data line of said faulty CAM cell to a logical one; and setting a complementary search data line of said faulty CAM cell to a logical zero; identifying a stuck open fault with a transistor having a gate coupled to a mask register, if said match line is set to logical one (M_2 S-Open line 1). The circuit of Wright associates the mask register with the M_2 transistor. Motivation for Wright comes from test algorithms used with ternary (internally maskable) CAMs (see Abstract and Introduction). One with ordinary skill in

the art at the time of the invention, motivated as suggested, would have found it obvious to apply the techniques of Wright with Zhao #1, #2 and Patel in order to include testing relationships to masking. And in view of the motivation and design choice previously stated, the claim is rejected.

As per Claim 20:

Zhao #1 Table 3 further teaches the method of claim 1, wherein said step of applying at least one signal comprises: setting a storage location of said faulty CAM cell to a logical zero; setting a mask value of said faulty CAM cell to a logical one; setting a search data line of said faulty CAM cell to a logical zero; setting a complementary search data line of said faulty CAM cell to a logical one; and identifying a stuck open fault with a transistor having a gate coupled to a mask register, if said match line is set to logical one (M_1 S-Open line 2). The circuit of Wright (M5) associates the mask register with the M_1 transistor. And in view of the motivation and design choice previously stated, the claim is rejected.

As per Claim 21:

Zhao #1 Table 3 further teaches the method of claim 1, wherein said step of applying at least one signal comprises: setting a storage location of said faulty CAM cell to a logical zero; setting a mask value of said faulty CAM cell to a logical one; setting a search data line of said faulty CAM cell to a logical one; setting a complementary search data line of said faulty CAM cell to a logical zero; and identifying a short circuit fault with a transistor having a gate coupled to a mask register, if said match line is set to logical zero (M_2 S-On line 1). The circuit of Wright (M2) associates the mask register with the

M_2 transistor. And in view of the motivation and design choice previously stated, the claim is rejected.

As per Claim 22:

Zhao #1 Table 3 further teaches the method of claim 1, wherein said step of applying at least one signal comprises: setting a storage location of said faulty CAM cell to a logical zero; setting a mask value of said faulty CAM cell to a logical zero; setting a search data line of said faulty CAM cell to a logical zero; setting a complementary search data line of said faulty CAM cell to a logical one; and identifying a short circuit fault with a transistor having a gate coupled to a mask register, if said match line is set to logical zero(M_2 S-On line 2). The circuit of Wright (M2) associates the mask register with the M_2 transistor. And in view of the motivation and design choice previously stated, the claim is rejected.

12. Claim 3, 23 and 24-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaginele, U.S. Patent Application No. 2005/0050408, Zhao et al., (herein Zhao #1), "Testing SRAM-Based Content Addressable Memories", in view of Zhao et al. (herein Zhao #2), U.S. Patent No. 6496950, and further in view of Patel, "Circuits for Low Power Traffic Encoding".

As per Claim 23:

Kaginele teaches a system for testing a CAM device (see Title) comprising: an interface for sending and receiving signals from the CAM device (FIG.8 502 and 504); and a processor (FIG.8 532), coupled to said interface (see FIG.8), for controlling

signals that are sent to the CAM device (FIG.8 534, 536, and FIG.3 300) and for reading signals received from the CAM device (see paragraph [0070], wherein said processor operates said interface to test said CAM device (see Title), but fails to specify the tests as claimed by the applicant. But the analogous art of Zhao #1 teaches a system for testing a (CAM) device (see Title), comprising testing said CAM device for stuck match lines (see page 1061, pass 3 and page 1062 column 1 bullet 5 or column 2 bullet 9); but is not very specific about testing for weak pull-downs. But in the analogous art of Zhao #2, the feature is disclosed, wherein there is (b) testing said CAM device for weak-pull down lines (see column 13 lines 50-67 and column 14 lines 1-22); and further, (c) testing each CAM cell in said CAM device to locate a faulty CAM cell (column 14 lines 54-67 and column 15 lines 1-22); but Zhao #2 fails to further teach diagnosing faults. But Zhao #1 further teaches this feature wherein (d) for each faulty CAM cell identified in step (c) (comparison related faults, page 1057 column 1 4.2 1st paragraph), diagnosing a cause of fault for said faulty CAM cell by applying at least one signal and reading a state of a match line associated with said faulty cell (see Tables 2 and 3 on page 1058). The examiner, being one of ordinary skill, recognizes the difference between the above references and the application to be simply a difference between the level of the match line (ML) under the test condition of a "match": The references teach that ML=1=Match, but this application teaches that ML=0=Match. But such a difference is an obvious alternative choice of design (see Patel on page 4 column 1 last paragraph). Therefore, no differences exist between the references and the application, when viewed in light of such a design choice. And in Zhao #1, the Abstract cites an

advantage to be complete characterization of comparison faults is attained by analysis of the circuit structure: In Zhao #2, the advantage stated is a testing procedure for locating faults in a comparison section. In Patel, the design choice is driven (page 4 column 1 last paragraph) by a choice of using ML=0=Match to conserve power. One with ordinary skill in the art at the time of the invention, motivated as suggested, would have found it obvious to test for faults in the comparison section, and to use the design choice of ML=0=Match (in Patel) to conserve power, and also to use the diagnosis tables of Zhao #1 in order to improve test results in Zhao #2.

As per Claims 3 and 24:

Kaginele further teaches the method and system of claims 1 and 23, wherein said step of applying at least one signal comprises: setting a mask value (paragraph [0007]) of said faulty CAM cell to a logical zero (see Claim 8); and identifying a faulty match line if said match line is set to logical zero (paragraph [0017]). And in view of the motivation previously stated, the claims are rejected.

As per Claim 25:

Zhao #1 teaches the system of claim 23, wherein said processor applying at least one signal comprises: setting a storage location of said faulty CAM cell to a logical zero; setting a search data line of said faulty CAM cell to a logical one; setting a complement search data line of said faulty CAM cell to a logical zero; and identifying a faulty match line if said match line is set to logical zero (Table 3 ML S-A-0 line 2).

NOTE: In view of the design choice where ML=0=Match is chosen (see Claim 1 above),

the references used in Zhao #1 Table 3 are equivalent to the applicant's Table 1 as follows:

S = D in applicant's Table 1.

S' = D# in applicant's Table 1.

CBL' = SD in applicant's Table 1 (Complementing enables ML=0=Match).

CBL = SD# in applicant's Table 1 (Complementing enables ML=0=Match).

ML Good/Fail = ML Fault-Free/Faulty in applicant's Table 1.

In view of the applicant's paragraphs [0009] and [0010], the Mask register is assumed on all the time when testing faults, and thus the binary CAM in Zhao #1 applies in such a case. And in view of the motivation previously stated, the claim is rejected.

As per Claim 26:

Zhao #1 teaches the system of claim 23, wherein said processor applying at least one signal comprises: setting a storage location of said faulty CAM cell to a logical one; setting a search data line of said faulty CAM cell to a logical zero; setting a complement search data line of said faulty CAM cell to a logical one; and identifying a faulty match line if said match line is set to logical zero (Table 3 ML S-A-0 line 1). And in view of the motivation and design choice previously stated, the claim is rejected.

As per Claim 27:

Zhao #1 Table 3 further teaches the system of claim 23, wherein said processor applies said at least one signal comprises: setting a storage location of said faulty CAM cell to a logical zero; setting a mask value of said faulty CAM cell to a logical one; setting a search data line of said faulty CAM cell to a logical zero; setting a complement

search data line of said faulty CAM cell to a logical one; and identifying a faulty match line if said match line is set to logical one (Table 3 ML S-A-1 line 2). And in view of the motivation and design choice previously stated, the claim is rejected.

As per Claim 28:

Zhao #1 Table 3 further teaches the system of claim 23, wherein said processor applies said at least one signal comprises: setting a storage location of said faulty CAM cell to a logical one; setting a mask value of said faulty CAM cell to a logical one; setting a search data line of said faulty CAM cell to a logical one; setting a complementary search data line of said faulty CAM cell to a logical zero; and identifying a faulty search data line if said match line is set to logical one (Table 3 CBL' S-A-0). And in view of the motivation and design choice previously stated, the claim is rejected.

As per Claim 29:

Zhao #1 Table 3 further teaches the system of claim 23, wherein said processor applies said at least one signal comprises: setting a storage location of said faulty CAM cell to a logical one; setting a mask value of said faulty CAM cell to a logical one; setting a search data line of said faulty CAM cell to a logical zero; setting a complementary search data line of said faulty CAM cell to a logical one; and identifying a faulty search data line if said match line is set to logical zero (Table 3 CBL' S-A-1). And in view of the motivation and design choice previously stated, the claim is rejected.

As per Claim 30:

Zhao #1 Table 3 further teaches the system of claim 23, wherein said processor applies said at least one signal comprises: setting a storage location of said faulty CAM

cell to a logical zero; setting a mask value of said faulty CAM cell to a logical one; setting a search data line of said faulty CAM cell to a logical zero; setting a complementary search data line of said faulty CAM cell to a logical one; and identifying a faulty complement search data line if said match line is set to a logical one (Table 3 CBL S-A-0). And in view of the motivation and design choice previously stated, the claim is rejected.

As per Claim 31:

Zhao #1 Table 3 further teaches the system of claim 23, wherein said processor applies said at least one signal comprises: setting a storage location of said faulty CAM cell to a logical zero; setting a mask value of said faulty CAM cell to a logical one; setting a search data line of said faulty CAM cell to a logical one; setting a complementary search data line of said faulty CAM cell to a logical zero; and identifying a faulty complement search data line if said match line is set to logical zero (Table 3 CBL S-A-1). And in view of the motivation and design choice previously stated, the claim is rejected.

As per Claim 32:

Zhao #1 Table 3 further teaches the system of claim 23, wherein said processor applies said at least one signal comprises: setting a storage location of said faulty CAM cell to a logical one; setting a mask value of said faulty CAM cell to a logical one; setting a search data line of said faulty CAM cell to a logical one; setting a complementary search data line of said faulty CAM cell to a logical zero; and identifying an stuck open fault with a transistor having a gate coupled to a data storage node of said CAM cell, if

said match line is set to logical one (M_2 S-Open line 1). And in view of the motivation and design choice previously stated, the claim is rejected.

As per Claim 33:

Zhao #1 Table 3 further teaches the system of claim 23, wherein said processor applies said at least one signal comprises: setting a storage location of said faulty CAM cell to a logical zero; setting a mask value of said faulty CAM cell to a logical one; setting a search data line of said faulty CAM cell to a logical one; setting a complementary search data line of said faulty CAM cell to a logical zero; and identifying an short circuit fault with a transistor having a gate coupled to a data storage node of said CAM cell, if said match line is set to logical zero (M_2 S-On line 1). And in view of the motivation and design choice previously stated, the claim is rejected.

As per Claim 34:

Zhao #1 Table 3 further teaches the system of claim 23, wherein said processor applies said at least one signal comprises: setting a storage location of said faulty CAM cell to a logical zero; setting a mask value of said faulty CAM cell to a logical one; setting a search data line of said faulty CAM cell to a logical zero; setting a complementary search data line of said faulty CAM cell to a logical one; and identifying an stuck open fault with a transistor having a gate coupled to a complement of a data storage node if said match line is set to a logical one (M_1 S-Open line 2). And in view of the motivation and design choice previously stated, the claim is rejected.

As per Claim 35:

Zhao #1 Table 3 further teaches the system of claim 23, wherein said processor applies said at least one signal comprises: setting a storage location of said faulty CAM cell to a logical one; setting a mask value of said faulty CAM cell to a logical one; setting a search data line of said faulty CAM cell to a logical zero; setting a complementary search data line of said faulty CAM cell to is set to a logical one; and identifying a short circuit fault with a transistor having a gate coupled to a complement of a data storage node, if said match line is set to logical zero (M_1 S-On line 2). And in view of the motivation and design choice previously stated, the claim is rejected.

As per Claim 36:

Zhao #1 Table 3 further teaches the system of claim 23, wherein said processor applies said at least one signal comprises: setting a storage location of said faulty CAM cell to a logical zero; setting a mask value of said faulty CAM cell to a logical one; setting a search data line of said faulty CAM cell to a logical zero; setting a complementary search data line of said faulty CAM cell to a logical one; and identifying a stuck open fault with a transistor having a gate coupled to a search data line, if said match line is set to logical one (M_2 S-On line 2). And in view of the motivation and design choice previously stated, the claim is rejected.

As per Claim 37:

Zhao #1 Table 3 further teaches the system of claim 23, wherein said processor applies said at least one signal comprises: setting a storage location of said faulty CAM cell to a logical zero; setting a mask value of said faulty CAM cell to a logical one; setting a search data line of said faulty CAM cell to a logical zero; setting a

complementary search data line of said faulty CAM cell to a logical one; and identifying a short circuit fault with a transistor having a gate coupled to a search data line, if said match line is set to logical one (M_1 S-On line 1). And in view of the motivation and design choice previously stated, the claim is rejected.

As per Claim 38:

Zhao #1 Table 3 further teaches the system of claim 23, wherein said processor applies said at least one signal comprises: setting a storage location of said faulty CAM cell to a logical zero; setting a mask value of said faulty CAM cell to a logical one; setting a search data line of said faulty CAM cell to a logical zero; setting a complementary search data line of said faulty CAM cell to a logical one; and identifying a stuck open fault with a transistor having a gate coupled to a complementary search data line, if said match line is set to one (M_1 S-Open line 2). And in view of the motivation and design choice previously stated, the claim is rejected.

As per Claim 39:

Zhao #1 Table 3 further teaches the system of claim 23, wherein said processor applies said at least one signal comprises: setting a storage location of said faulty CAM cell to a logical zero; setting a mask value of said faulty CAM cell to a logical one; setting a search data line of said faulty CAM cell to a logical one; setting a complementary search data line of said faulty CAM cell to a logical zero; and identifying a short circuit fault with a transistor having a gate coupled to a complementary search data line, if said match line is set to logical zero (M_2 S-On line 1). And in view of the motivation and design choice previously stated, the claim is rejected.

13. Claims 40-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaginele, U.S. Patent Application No. 2005/0050408, Zhao et al., (herein Zhao #1), "Testing SRAM-Based Content Addressable Memories", in view of Zhao et al. (herein Zhao #2), U.S. Patent No. 6496950, in view of Patel, "Circuits for Low Power Traffic Encoding", and further in view of Wright et al. (herein Wright), "Transistor-Level Fault Analysis and Test Algorithm Development for Ternary Dynamic Content Addressable Memories".

As per Claim 40:

Zhao #1 Table 3 further teaches the system of claim 23, wherein said processor applies said at least one signal comprises: setting a storage location of said faulty CAM cell to a logical one; setting a mask value of said faulty CAM cell to a logical one; setting a search data line of said faulty CAM cell to a logical one; and setting a complementary search data line of said faulty CAM cell to a logical zero; identifying a stuck open fault with a transistor having a gate coupled to a mask register, if said match line is set to logical one (M_2 S-Open line 1). The circuit of Wright associates the mask register with the M_2 transistor. Motivation for Wright comes from test algorithms used with ternary (internally maskable) CAMs (see Abstract and Introduction). One with ordinary skill in the art at the time of the invention, motivated as suggested, would have found it obvious to apply the techniques of Wright with Zhao #1, #2 and Patel in order to include testing, relationships to masking. And in view of the motivation and design choice previously stated, the claim is rejected.

As per Claim 41:

Zhao #1 Table 3 further teaches the system of claim 23, wherein said processor applies said at least one signal comprises: setting a storage location of said faulty CAM cell to a logical zero; setting a mask value of said faulty CAM cell to a logical one; setting a search data line of said faulty CAM cell to a logical zero; setting a complementary search data line of said faulty CAM cell to a logical one; and identifying a stuck open fault with a transistor having a gate coupled to a mask register, if said match line is set to logical one (M_1 S-Open line 2). The circuit of Wright (M5) associates the mask register with the M_1 transistor. And in view of the motivation and design choice previously stated, the claim is rejected.

As per Claim 42:

Zhao #1 Table 3 further teaches the system of claim 23, wherein said processor applies said at least one signal comprises: setting a storage location of said faulty CAM cell to a logical zero; setting a mask value of said faulty CAM cell to a logical one; setting a search data line of said faulty CAM cell to a logical one; setting a complementary search data line of said faulty CAM cell to a logical zero; and identifying a short circuit fault with a transistor having a gate coupled to a mask register, if said match line is set to logical zero (M_2 S-On line 1). The circuit of Wright (M2) associates the mask register with the M_2 transistor. And in view of the motivation and design choice previously stated, the claim is rejected.

As per Claim 43:

Zhao #1 Table 3 further teaches the system of claim 23, wherein said processor applies said at least one signal comprises: setting a storage location of said faulty CAM cell to a logical zero; setting a mask value of said faulty CAM cell to a logical zero; setting a search data line of said faulty CAM cell to a logical zero; setting a complementary search data line of said faulty CAM cell to a logical one; and identifying a short circuit fault with a transistor having a gate coupled to a mask register, if said match line is set to logical zero(M_2 S-On line 2). The circuit of Wright (M2) associates the mask register with the M_2 transistor. And in view of the motivation and design choice previously stated, the claim is rejected.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P. Trimmings whose telephone number is (571) 272-3830. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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